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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,852	09/25/2003	Toshiyuki Kasai	117024	4391

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,852	KASAI, TOSHIYUKI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 January 2007 has been entered. Claims 1-29 are pending.

Election/Restrictions

2. Newly submitted claim 29 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claim 29 is drawn to Figure 5, whereas claims 1-28 are drawn to Figure 3. The inventions shown in Figure 3 and Figure 5 are directed to related species. The related inventions are distinct if the (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant

case, the inventions as claimed cannot be used together since they are different circuit structures for pixels, and therefore are not capable of being used together.

Furthermore, the inventions as claimed do not encompass overlapping subject matter and there is nothing of record to show them to be obvious variants.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 29 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

3. Claims 1, 5, 14 and 18 are objected to because of the following:

The claims recite the limitation "at least one of the first circuit unit and the second circuit unit including a plurality of transistors connected in series or in parallel." Figure 3, however, only shows that the first circuit unit containing transistors connected in parallel and the second circuit unit containing transistors connected in series. Therefore, based on the wording of the claim limitation, at least one of the first and second circuit units has transistors in series or parallel, however, the specification does not allow for the choice between parallel or series. For example, if the examiner chose the second circuit unit, the limitation would require it to have transistors in either parallel or series, but Figure 3 shows only the second circuit having transistors in series and therefore having them in parallel has not been disclosed as an option and cannot be

claimed. Furthermore, the examiner suggests changing the word "including" in the claim to "includes" for grammatical reasons.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5-14, 16 and 18-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Yumoto (US 2005/0200300).

Regarding claims 1, Yumoto discloses an electronic circuit, comprising:

a first circuit unit (Figure 8 shows a first circuit unit made up of TFT1) through which a first current having a first current level passes (Paragraph [0065] explains that current level I_w passes through TFT1.);

a capacitor element (Figure 8, C) to store a quantity of electric charge corresponding to the first current level (Paragraph [0064] explains that capacitor C holds the voltage created at the gate of the first transistor TFT1.); and

a second circuit unit (Figure 8 shows a second circuit made up of TFT2a and TFT2b.) to generate a second current (Paragraph [0067] explains that the current generated at the second circuit is the drive current I_{drv}.) having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (Paragraph [0067] explains that the drive current is generated based on the charge stored in the capacitor, while paragraph [0068]-[0069] explain that the first and second current levels are proportional and that depending on the circumstances, such as the desired drive current and the design characteristics of the transistors, the current levels can be different.),

at least one of the first circuit unit and the second circuit unit including a plurality of transistors connected in series or in parallel (Figure 8 shows that the second circuit unit contains transistors TFT2a and TFT2b which are connected in series, see also paragraph [0073].),

respective gates of the transistors being mutually connected (Figure 8 shows that the gates of the transistors are connected together.),

the first circuit and the second circuit unit constituting a current mirror circuit (Paragraph [0066] explains that the first and second circuits form a current mirror circuit.).

Regarding claim 3, please refer to the rejection of claim 1 where it is explained that the second circuit includes a plurality of transistors connected in series (Figure 8).

Regarding claim 5, please refer to the rejection of claim 1, and furthermore Yumoto also discloses that the electrical connections of the plurality of transistors is controlled by a control element (Figure 8 and paragraph [0067] explain how TFT4 acts to control the electrical connections of the transistors TFT2a and TFT2b.).

Regarding claim 14, please refer to the rejection of claim 1, and furthermore Yumoto also discloses and electronic device provided with a first signal line (Figure 2, scan1), a second signal line (Figure 2, data), and a plurality of unit circuits (Figure 2, 25 PIXELs), each of the plurality of unit circuits comprising:

a switching elements connected to the first signal line (Figure 8 shows TFT3), and on/off state of the switching element being controlled by switching signals supplied from the first signal line (Figure 8 shows that the gate of TFT3 is controlled by scanA.);

a first circuit unit connected to the second signal line (Figure 8 shows that TFT1 is connected to the line data through TFT3.), a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element (Paragraph [0065] explains that current level I_w passes through TFT1, where I_w is seen in Figure 8 to be flowing from the data line.); and

a capacitor and second circuit unit as described in the rejection of claim 1 (see Figure 8).

Regarding claim 16, please refer to the rejection of claims 1 and 14 where it is explained that the second circuit includes a plurality of transistors connected in series (Figure 8).

Regarding claim 18, please refer to the rejection of claim 14, and furthermore Yumoto also discloses that the electrical connections of the plurality of transistors is controlled by a control element (Figure 8 and paragraph [0067] explain how TFT4 acts to control the electrical connections of the transistors TFT2a and TFT2b.)

Regarding claims 6 and 19, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where at least one of the plurality of transistors being a transistor common to the first circuit unit and the second circuit unit (Figure 8 shows that that at least one of the plurality of transistors is common to the first and second circuit units.).

Regarding claims 7 and 20, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where the plurality of transistors have the same driving capability (Paragraph [0027] explains that the transistors have the same driving capability.).

Regarding claims 8 and 21, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where the plurality of transistors being formed in a bundle

(Figure 8, where the transistors here are considered "bundled" since they are close together).

Regarding claims 9 and 22, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where the first current level is higher than the second current level (Paragraph [0069] explains of an example where I_w is higher than I_{drv}.).

Regarding claims 10 and 23, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where the second current level is higher than the first current level (Paragraphs [0068]-[0069] explain that the values W1, W2, L1 and L2 can be chosen, meaning that these values can be chosen to make a case where I_w is lower than I_{drv}, therefore making the second current higher than the first.).

Regarding claims 11 and 24, Yumoto discloses the electronic circuit and device according to claims 1 and 14, where there are electronic elements being supplied with the second current (Figure 8 shows the electronic element OLED).

Regarding claims 12 and 25, Yumoto discloses the electronic circuit and device according to claims 11 and 24,where the electronic elements is an electro-optical element or a current-driven element (Paragraph [0067], at the end explains that OLED is current driven.).

Regarding claims 13 and 26, Yumoto discloses the electronic circuit and device according to claims 12 and 25, where the electronic element is an organic EL element (Paragraph [0064] explains that the light emitting element is made of an organic EL element.).

Regarding claims 27 and 28, Yumoto discloses an electronic apparatus having mounted therein the electronic circuit and device of claims 1 and 14 (Figure 2 shows that all circuits and devices, shows as PIXEL 25, are mounted in the display, also see paragraph [0001].).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,909,242).

Regarding claim 2, Kimura discloses an electronic circuit, comprising:

a first circuit unit (Figure 19, transistor 1907) through which a first current having a first current level passes (Figure 20A shows that current I_2 flows through transistor 1907.);

a capacitor element (Figure 19, item 1909) to store a quantity of electric charge corresponding to the first current level (Column 6, lines 25-53 explain that electric charge stored in the capacitor is equal to I_2 at the end of the charging procedure [towards the end of the passage].);

a second circuit unit (Figure 19, transistor 1908) to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (Figure 20C shows I_{EL} that flows through transistor 1908, where the current level will be different based upon the specifications of the transistors 1907 and 1908 as explain in column 6, lines 62-67.), and

the first circuit unit and the second circuit unit constituting a current mirror circuit (Column 6, lines 57-58).

Kimura does not explicitly teach that the first circuit unit of Figure 19 includes a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected.

However, Kimura does teach a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected (Fig. 27B, see column 43, lines 27-35, and see column 43, lines 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the parallel transistors of Kimura into the first circuit of Kimura's embodiment in Figure 19 in order to have a method of further limiting possible display irregularities from developing.

Regarding claim 15, please refer to the rejection of claim 2, and furthermore Kimura also discloses and electronic device provided with a first signal line (Figure 19, item 1902), a second signal line (Figure 19, item 1901), and a plurality of unit circuits (Figure 3A), each of the plurality of unit circuits comprising:

a switching elements connected to the first signal line (Figure 19, transistor 1905), and on/off state of the switching element being controlled by switching signals supplied from the first signal line (Figure 19 shows that gate line 1902 is connected to the gate of transistor 1905, thus determining when it is turned on.);

a first circuit unit connected to the second signal line (Figure 19 shows that transistor 1907 is connected to line 1901 through transistor 1905), a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element (Column 6, lines 25-53 explain that electric charge stored in the capacitor is equal to I_2 at the end of the charging procedure [towards the end of the passage], where I_2 is equal to I_{data}.); and

a capacitor and second circuit unit as described in the rejection of claim 2 (Figure 19).

7. Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,909,242) in view of Yumoto (US 2005/0200300).

Regarding claim 4, Kimura discloses an electronic circuit, comprising:

a first circuit unit (Figure 19, transistor 1907) through which a first current having a first current level passes (Figure 20A shows that current I_2 flows through transistor 1907.);

a capacitor element (Figure 19, item 1909) to store a quantity of electric charge corresponding to the first current level (Column 6, lines 25-53 explain that electric charge stored in the capacitor is equal to I_2 at the end of the charging procedure [towards the end of the passage].);

a second circuit unit (Figure 19, transistor 1908) to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (Figure 20C shows I_{EL} that flows through transistor 1908, where the current level will be different based upon the specifications of the transistors 1907 and 1908 as explain in column 6, lines 62-67.), and

the first circuit unit and the second circuit unit constituting a current mirror circuit (Column 6, lines 57-58).

Kimura does not explicitly teach that the first circuit unit of Figure 19 includes a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected.

However, Kimura does teach a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected (Fig. 27B, see column 43, lines 27-35, and see column 43, lines 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the parallel transistors of Kimura into the first circuit of Kimura's embodiment in Figure 19 in order to have a method of further limiting possible display irregularities from developing.

Kimura fails to teach that the second circuit unit includes a plurality of transistors connected in series with respective gates of the second circuit unit transistors being mutually connected.

Yumoto discloses of a second circuit unit that includes a plurality of transistors connected in series with respective gates of the second circuit unit transistors being mutually connected (Figure 8 shows a second circuit made up of TFT2a and TFT2b, where the gates are connected and the transistors are in series.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention wad made to make the second circuit taught by Kimura have two transistors connected in series as taught by Yumoto in order to suppress the leakage current which forms when having only one transistor such that display defects can be prevented (See paragraph [0073] of Yumoto.).

Regarding claim 17, please refer to the rejection of claim 4, and furthermore Yumoto also discloses and electronic device provided with a first signal line (Figure 2,

scan1), a second signal line (Figure 2, data), and a plurality of unit circuits (Figure 2, 25 PIXELs), each of the plurality of unit circuits comprising:

a switching elements connected to the first signal line (Figure 8 shows TFT3), and on/off state of the switching element being controlled by switching signals supplied from the first signal line (Figure 8 shows that the gate of TFT3 is controlled by scanA.);

a first circuit unit connected to the second signal line (Figure 8 shows that TFT1 is connected to the line data through TFT3.), a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element (Paragraph [0065] explains that current level I_w passes through TFT1, where I_w is seen in Figure 8 to be flowing from the data line.); and

a capacitor and second circuit unit as described in the rejection of claim 4 (see Figure 8 of Yumoto and Figure 19 of Kimura).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nishitoba et al. (US 2002/0196212) disclose of a pixel circuit in which transistors are connected in series in order to mitigate the influence of variations between transistors that make up a current mirror circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

9 February 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER